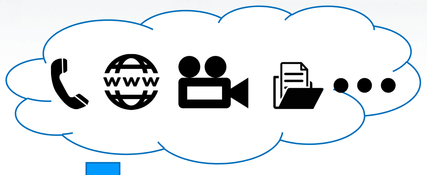
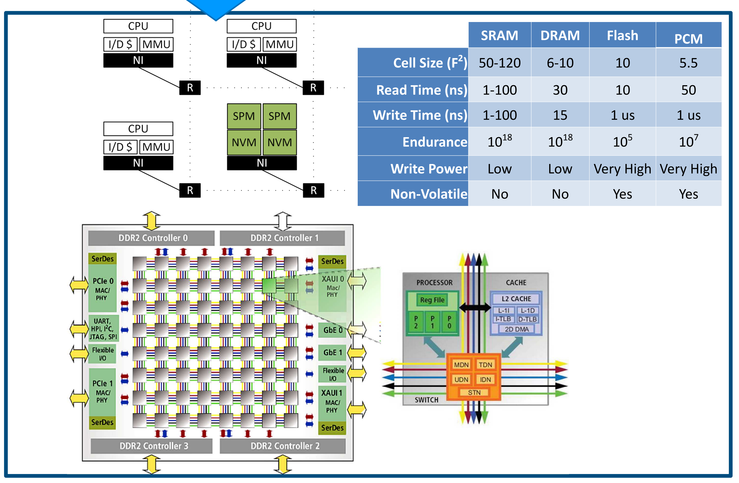
Characterizing and Exploiting Phasic Memory Behavior for Many-Core Architectures

Bryan Donyanavard and Nikil Dutt
Dept. of Computer Science, UC Irvine
www.duttgroup.ics.uci.edu
bdonyana@uci.edu



Variable Target Architectures

- Heterogeneous embedded architectures and memory organizations
  - Cache, SPMs, NVMs, a combination…
- Workload variability
  - Unpredictable – tasks coming and going
  - Memory behavior within applications

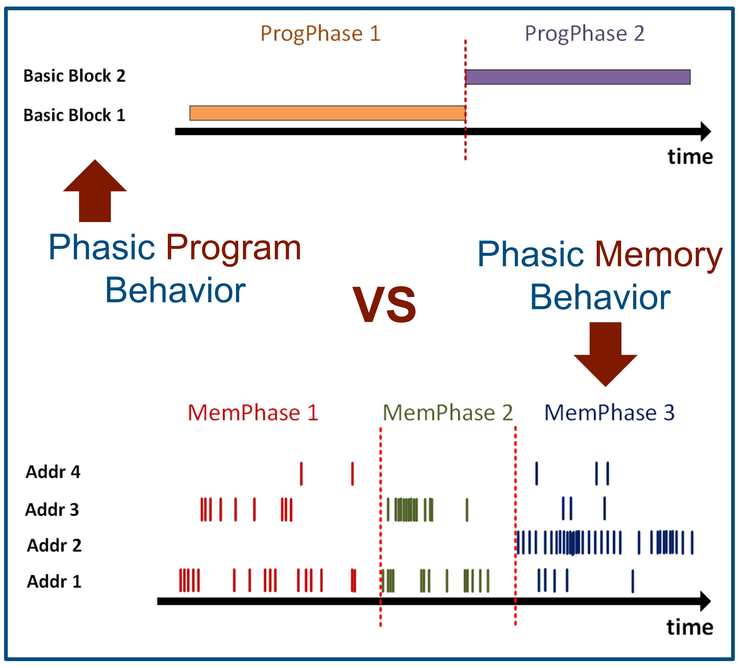


	SRAM	DRAM	Flash	PCM
Cell Size (F^2)	50-120	6-10	10	5.5
Read Time (ns)	1-100	30	10	50
Write Time (ns)	1-100	15	1 us	1 us
Endurance	10^{18}	10^{18}	10^{5}	10^{7}
Write Power	Low	Low	Very High	Very High
Non-Volatile	No	No	Yes	Yes

Embedded Systems Architectures

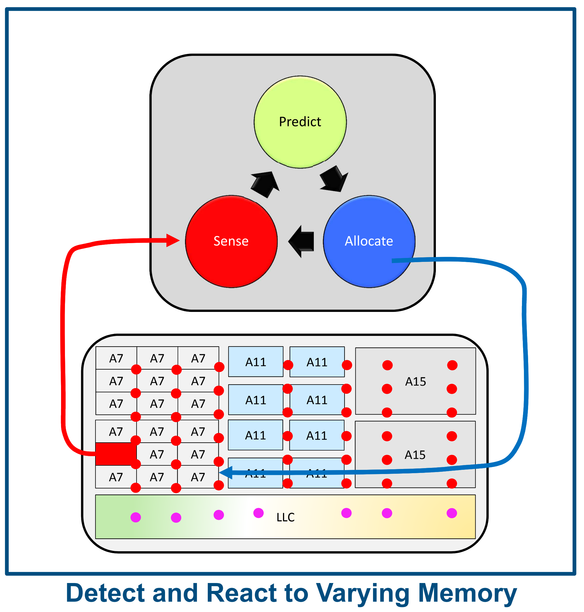
Phasic Memory Behavior

- Memory access pattern of benchmark may change drastically over course of execution
- Difficult to extract from existing benchmarks
  - Restricted by simulated inputs and target architecture
  - Requires storage of HUGE amount of data
- Necessary to leverage for memory management techniques
- Phasic program behavior != phasic memory behavior

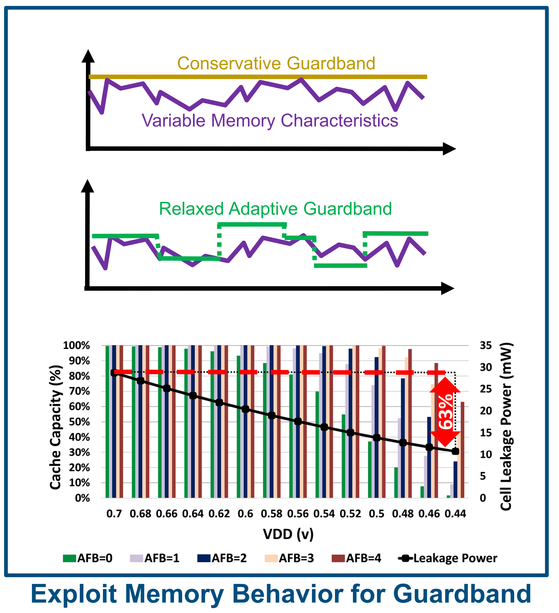


What We Need

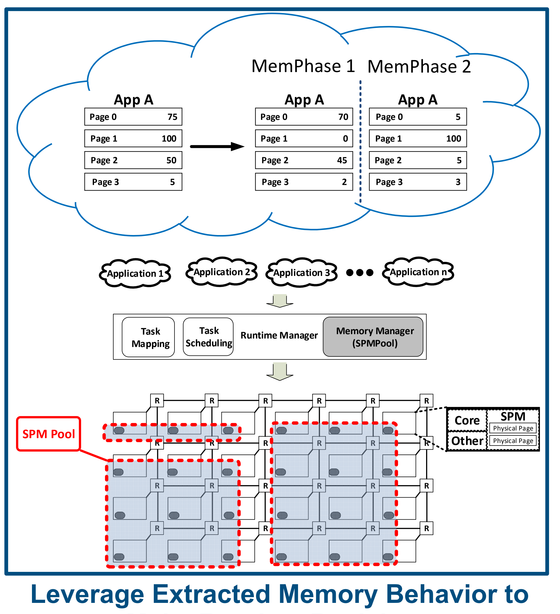
- Structure and technique to extract and represent memory access pattern
  - Compact
  - Input-adverse



Detect and React to Varying Memory Requirements



Exploit Memory Behavior for Guardband Relaxation



Leverage Extracted Memory Behavior to Make Runtime Decisions